

REMARKS

Claims 27-46 and 72, 73 and 75-95 are pending in the present application. Claims 28, 31, 38, 72, 76, 77, 84, 90 and 95 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

The applicants note, with appreciation, that the Office Action indicates at page 2, paragraph 1, that claims 27-46 are allowed. The applicants note that claim 95 is dependent from allowed claim 27 and is believed to be allowable. Allowance of claim 95 is respectfully requested.

Claims 72-73, 75-83 and 87-89 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama (U.S. Patent Number 6,548,875). Claims 84-86 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama in view of Liu (U.S. Patent Number 6,528,847). Claim 90 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiyama in view of Lee, *et al.* (U.S. Patent Number 6,376,318). The applicants note that claims 93 and 94 are listed as being rejected in the Office Action Summary; however, there is no specific rejection of these claims in the Detailed Action. Reconsideration of the rejection and allowance of claims 72, 73 and 75-94 are respectfully requested.

In the present invention as claimed in claim 72, a MOS transistor having elevated source and drain structures includes a “gate electrode” on a “gate dielectric layer”, the “gate dielectric layer includes a horizontal portion that extends across a bottom portion of the gate electrode and side portions that extend in a vertical direction along lower side portions of the gate electrode”, and “an epitaxial layer contacting the side portions of the gate dielectric layer on the substrate and extending from a point of contact with the side portions of the gate dielectric layer substantially parallel to the substrate in a horizontal direction”.

Nishiyama discloses an SiO<sub>2</sub> film 514 formed on a first dielectric film 504 extending under the SiO<sub>2</sub> film 514 and gate sidewalls 508 that extend over the entire

sidewalls of the SiO<sub>2</sub> film 514. Source/drain semiconductor layers 509, 510 contact bottom corners of the gate sidewalls 508 and extend from the bottom corners of the gate sidewalls 508 at an angle.

Nishiyama fails to teach or suggest a MOS transistor having elevated source and drain structures that includes “an epitaxial layer contacting the side portions of the gate dielectric layer on the substrate and extending from a point of contact with the side portions of the gate dielectric layer substantially parallel to the substrate in a horizontal direction”, as claimed in claim 72. Instead, in Nishiyama, the portion of the source/drain semiconductor layers 509, 510 contacting the bottom corners of the gate sidewalls 508 extend from the bottom corners of the gate sidewalls 508 at an angle. Further, Nishiyama fails to teach or suggest a MOS transistor having elevated source and drain structures that includes “a gate dielectric layer that includes a horizontal portion that extends across a bottom portion of the gate electrode and side portions that extend in a vertical direction along lower side portions of the gate electrode”, as claimed in claim 72. Similar to the applicants’ admitted prior art of Figures 1 and 2 in which insulative spacers 118, 218 are formed on the sidewalls of the gate structure 110, 210 and the gate dielectric 112, 212 are formed below the gate structure 110, 210, the Nishiyama gate spacers 508 are formed on the sidewalls of the SiO<sub>2</sub> film 514 and the first dielectric film 504 is formed below the SiO<sub>2</sub> film 514. The gate sidewalls 508 of Nishiyama at side portions of the gate are not a “gate dielectric layer”, as claimed, but rather, the gate sidewalls 508 of Nishiyama are sidewall spacers and do not insulate the gate from a channel region.

It is therefore submitted that independent claim 72 is allowable over Nishiyama. Reconsideration of the rejection of claim 72 under 35 U.S.C. 103(a) as being unpatentable over Nishiyama, and allowance of the claims, are respectfully requested. With regard to the rejection of dependent claims 73 and 75-92 as being unpatentable over Nishiyama, it follows that these claims should inherit the allowability of the independent claims from which they depend.

With regard to the rejection of claims 84-86 under 35 U.S.C. 103(a) as being unpatentable over Nishiyama and Liu, Liu is cited in the Office Action as disclosing a

recessed channel. Liu discloses a polysilicon gate 36 formed on gate oxide layer 34, and spacers 60 formed on the gate oxide layer 34. Liu fails to teach or suggest an epitaxial layer, thus, like Nishiyama, Liu further fails to teach or suggest a MOS transistor having elevated source and drain structures that includes “an epitaxial layer contacting the side portions of the gate dielectric layer on the substrate and extending from a point of contact with the side portions of the gate dielectric layer substantially parallel to the substrate in a horizontal direction”, as claimed in claims 84-86. Further, Liu fails to teach or suggest a MOS transistor having elevated source and drain structures that includes “a gate dielectric layer that includes a horizontal portion that extends across a bottom portion of the gate electrode and side portions that extend in a vertical direction along lower side portions of the gate electrode”, as claimed in claim 84-86.

Accordingly, it is submitted that the combination of Nishiyama and Liu fails to teach or suggest the invention as claimed in claims 84-86. Reconsideration of the rejection of claims 84-86 under 35 U.S.C. 103(a) as being unpatentable over Nishiyama and Liu, and allowance of the claims, are respectfully requested.

With regard to the rejection of claim 90 under 35 U.S.C. 103(a) as being unpatentable over Nishiyama and Lee, *et al.*, Lee, *et al.* is cited in the Office Action as disclosing an oxide film spacer 27. Lee, *et al.* discloses a nitride film spacer 28 formed adjacent the oxide film spacer 27 and a selective epitaxial growth film 29 which forms a self aligned epitaxial silicon sliver (SESS) C adjacent the oxide film spacer 27 and under the nitride film spacer 28.

Like Nishiyama, Lee, *et al.* fails to teach or suggest a MOS transistor having elevated source and drain structures that includes “an epitaxial layer contacting the side portions of the gate dielectric layer on the substrate and extending from a point of contact with the side portions of the gate dielectric layer substantially parallel to the substrate in a horizontal direction” as claimed in claim 90. Instead, in Lee, *et al.*, there is contact between a dielectric layer and the epitaxial layer. Further, Lee, *et al.* fails to teach or suggest a MOS transistor having elevated source and drain structures that includes “a gate dielectric layer that includes a horizontal portion that extends across a bottom


portion of the gate electrode and side portions that extend in a vertical direction along lower side portions of the gate electrode”, as claimed in claim 90. Accordingly, it is submitted that the combination of Nishiyama and Lee, *et al.* fails to teach or suggest the invention as claimed in claim 90. Reconsideration of the rejection of claim 90 under 35 U.S.C. 103(a) as being unpatentable over Nishiyama and Lee, *et al.*, and allowance of the claims, are respectfully requested.

**Closing Remarks**

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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